PATENT ABSTRACTS OF JAPAN

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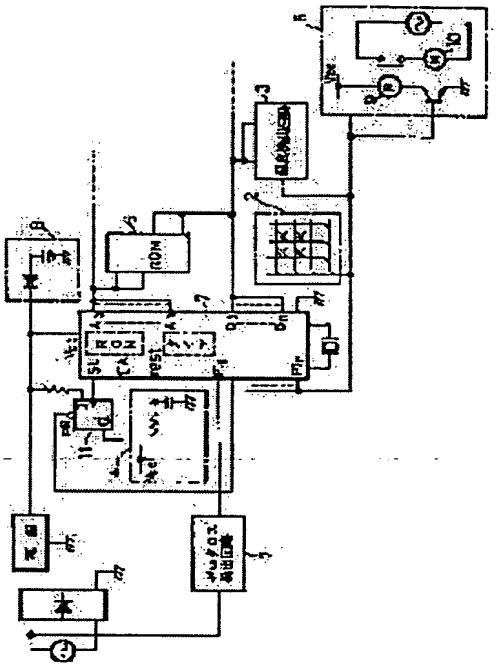
(54) STARTING METHOD FOR CONTROL PROGRAM

(57)Abstract:
PROBLEM TO BE SOLVED: To provide the starting method for a control program which can continue a process without altering the contents of a RAM memory even when a sleep mode is used in a power-OFF state.
SOLUTION: A one-chip microcomputer 7 which implements the sleep mode in the power-OFF state to save data necessary for resetting in a RAM memory is provided with an external ROM 6. In the ROM 6, a 2nd execution start address set on the downstream side of a RAM memory clear command in an initial processing routine that the microcomputer 7 executes at the time of resetting is written. The execution start address which has been written is read in when the power recovers to make usable the data saved in the RAM memory. When the power source is OFF, the process can be carried on even when the sleep mode is used.



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* NOTICES *

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CLAIMS

[Claim(s)]
[Claim 1] To the control equipment using the microcomputer which was made to perform the sleep mode which evacuates data required for a return at power off to a RAM memory, and saves data The 1st starting address which starts the initial setting which includes clear processing of a RAM memory at the time of starting, The 2nd starting address set up down-stream rather than clear processing of said RAM memory is prepared. The startup approach of a control program of having been made to perform processing after making said microcomputer acquiring the 2nd starting address at the time of discharge of a sleep mode and being based on the address.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the startup approach of the control program in the control equipment which used the microcomputer.
[0002]
[Description of the Prior Art] Generally, by the electronics control device using a microcomputer, in case a system is started, it is necessary to perform initialization (initialization) processing.
[0003] Initialization processing is for starting a system by setting up the port and peripheral LSI for [various] I/O, or clearing a RAM memory according to a system, (check).
[0004] Therefore, a reset circuit is prepared, when supply voltage starts on a guarantee electrical potential difference of operation, active [of the reset terminal of CPU] is carried out, and the address of a reset vector is made to read into CPU after powering on. The program for initialization is prepared for this starting address, and as shown in drawing 3 , after performing setting out of a port, setting out of various peripheral LSIs, the clearance (check) of a RAM memory, etc., the processing program of Maine is performed.
[0005] By the way, there are some which have the function to attain low-power-ization called a halt or sleep mode in a microcomputer in recent years.
[0006] For example, in the one chip microcomputer which contains circumference functions, such as RAM, ROM, an I/O Port, and a timer, in a one chip, if a halt or a sleep mode is performed, the internal clock of CPU will be suspended and the content of RAM or the register will be held. And since processing can be made to continue that after discharge in said mode is also at the held content, low-power-ization can be attained by using such the mode, when CPU does not process.
[0007]
[Problem(s) to be Solved by the Invention] However, when the above halts or sleep modes are used at the time of power off (a momentary stop, interruption to service, and switch-off are not asked), the problem which produces inconvenience is after power return.
[0008] That is, if the above-mentioned starting approach is used, since a reset circuit will work at the time of power return, the program for initialization will start and the content of the RAM memory will be cleared, in the thing he is trying to make the content set up with a switch memorize, processing is uncontinuable.
[0009] Although what is necessary is just to make it the program for initialization not start by the reset circuit at this time, when it is made such, there is a problem of initial starting becoming impossible.
[0010] Then, the technical problem of this invention is enabling it to continue processing, without changing the content of the RAM memory, even if it uses the mode called a halt or a sleep mode at the time of power off.
[0011]
[Means for Solving the Problem] In order to solve the above-mentioned technical problem, in claim 1, data required for a return at power off are evacuated to a RAM memory. The 1st starting address which starts the initial setting which includes clear processing of a RAM memory in the control equipment using the microcomputer which was made to perform the sleep mode which saves data at the time of a startup, The 2nd starting address set up down-stream rather than clear processing of said RAM memory is prepared. Said microcomputer was made to acquire the 2nd starting address at the time of discharge of a sleep mode, and the approach which was made to perform processing after being based on the address was adopted.
[0012] The content of the RAM memory is made not to be cleared by adopting such an approach by dividing and setting up the 1st starting address in the case of initial starting, and the 2nd starting address which a sleep mode is canceled [starting address] at the time of power return, and starts a program, and setting the 2nd starting address as the downstream rather than the check of a RAM memory at the time of power return.
[0013]
[Embodiment of the Invention] Hereafter, the gestalt of implementation of this invention is explained based on a drawing.
[0014] The control circuit of a sherbet feeder which used the starting approach of this invention for drawing 1 is shown.
[0015] a sherbet feeder makes the ice which manufactured ice with the freezer the shape of sherbet, and supplies it, and this control circuit is shown in drawing 1 — as — the zero cross detector 1, the switch matrix circuit 2, the temperature detector 3, a reset circuit 4, and the compressor actuation circuit 5 — it has ... and the composition that the exterior ROM 6 was connected to the one-chip microcomputer (the following, microcomputer) 7.
[0016] Moreover, the dc-battery is connected to the microcomputer 7 through diode as a backup power supply 8, and in case it is power off, power can be supplied to a microcomputer 7.
[0017] The zero cross detector 1 is the thing of the common knowledge which used the comparator, and when an alternating-voltage wave passes the zero point, it outputs a detecting signal to a microcomputer 7. With a microcomputer 7, based on the detecting signal, the sleep mode which detects power off and is later mentioned from the existence of a zero cross signal is performed, or frequency detection is performed from the period of a zero cross signal, and capacity setting out of the freezer according to a detection frequency etc. is performed.
[0018] The switch matrix circuit 2 is a switch for performing temperature setting out for example, using a membrane switch etc., and a microcomputer 7 reads setting out by the switch, and it memorizes the read content of setting out.
[0019] The temperature detector 3 consists of a temperature sensor and an A/D converter, changes into digital data the cooling

temperature of the freezer detected with the temperature sensor with an A/D converter, and inputs it into a microcomputer 7.
[0020] A reset circuit 4 is a well-known circuit as shown in drawing 1 , and inputs a reset signal into the reset terminal of a microcomputer 7 with ON of a power source.
[0021] To be shown in drawing 1 , the compressor actuation circuit 5 turns on and off the relay 9 for compressors of a freezer by the switching element by which microcomputer control was carried out, and can control a compressor 10 now.
[0022] A microcomputer 7 is what accumulated the Program ROM, Interior RAM, input/output port, timer/counter, serial I/O, and interruption circuit etc. on the same chip as CPU, and as shown in drawing 1 , it has the address bus A, data bus D, reset input rest, I/O Port PI, serial boat, and interruption input, the oscillation input terminal, etc. Moreover, the output of a system clock has also come be made by the built-in oscillator circuit by connecting vibrator, such as Xtal, at an oscillation input terminal.
[0023] Furthermore, the sleep mode status terminal SL and the program memory selection terminal EA are formed in the microcomputer 7. Said sleep mode status terminal SL is a terminal which tells that the microcomputer 7 became a sleep mode, and if a microcomputer 7 suspends the clock for interior actions and becomes a sleep mode, it will become active and it will be displayed. This sleep mode can be canceled by activating reset input rest.
[0024] It is a terminal for switching access to Built-in ROM and the exterior ROM 6, if the program memory selection terminal EA is made inactive, it will access Built-in ROM, and if it activates, it will access the exterior ROM 6.
[0025] With this gestalt, if the sleep mode status terminal SL and the program memory selection terminal EA are connected through latch 11 and said latch 11 cancels a sleep mode as shown in drawing 1 , the program memory selection terminal EA will be activated with a status signal, and access will be switched to the exterior ROM 6.
[0026] Moreover, it connects with I/O Port PI, and said latch makes the program memory selection terminal EA inactive, and enables it to have switched access to Built-in ROM by I/O Port PI at the time of sleep mode discharge.
[0027] That is, it is made to have used it, arranging Built-in ROM and the exterior ROM 6 to the same address (shadow), and switching with the program memory selection terminal EA.
[0028] Said interior ROM serves as a vector field, a monitor area, and a program field from the lower address (with this microcomputer, a start address is in low order) at order, as shown in drawing 2 .
[0029] As the address at the time of reset or interruption is written in and a vector field shows the lowest address (0000) at drawing 2 , the start address of an initial setting is written in as a reset vector as the 1st address.
[0030] An initial setting consists of routines, such as mode setting processing, a RAM clearance (RAM check), port setting out, timer setting out, a power line period judging, switch information reading, and temperature data reading, and initializes setting out for I/O and timer-related setting out, setting out of the power line period used by the main program, and reading of a switch, temperature setting out, etc.
[0031] The Maine processing performs processing at the time of power off etc. to processing and coincidence of the control of a freezer based on the parameter set up by the above-mentioned initial setting, reading of switch actuation, reading of temperature data, etc.
[0032] If the zero cross signal from a zero cross detector is detected and the input of a zero cross signal is lost, it will need to be processed at the time of a return at the time of said power off, for example, it will evacuate the data set up by the switch to Interior RAM, and will perform a sleep mode.
[0033] On the other hand, the program for the exterior ROM 6 to activate I/O Port PI with the start address of a power line period configuration routine at the time of sleep mode discharge, clear latch 11 from the least significant (0000) to the address, and make the program memory selection terminal EA inactive is written in.
[0034] This gestalt is constituted as mentioned above, and in initial starting at the time of switching on a power source first, a microcomputer 7 processes the mode setting routine which is the start address of an initial setting, as a start address is read and it is shown in (b) of drawing 2 by the reset signal from a reset circuit 4.
[0035] henceforth, order -- ->RAM clearance -> port setting-out -> timer setting-out -> -- it performs with ... and I/O and timer-related setting out is performed. The judgment and setting out of a power line period, a switch, temperature, etc. which are used by the main program are performed after it, and a main program is performed.
[0036] In a main program, the freezer based on setting out of an initial setting and processing of in addition to this actuation are performed, and the processing at the time of power off detects power off, such as interruption to service and hits.
[0037] If power off is now detected by the processing at the time of power off, a microcomputer 7 is required at the time of a return, for example, will evacuate the setting-out data based on a switch etc. to Interior RAM, will perform a sleep mode, and will activate the sleep mode status terminal SL. For this reason, the useful data under activation are saved in Interior RAM.
[0038] And as for a microcomputer 7, a sleep mode will be canceled by this reset signal, if a power source returns and a reset signal is inputted into a microcomputer 7 from a reset circuit 4. At this time, the output of the sleep mode status terminal EA is latched by the latch 11 who stood up previously, the program memory selection terminal SL becomes active, and the exterior ROM 6 is accessed.
[0039] Therefore, since the program memory selection terminal EA is made IAKUTIBU by the program which read the start address of a power line period judging routine, and was read simultaneously, a microcomputer 7 is jumped to a power line period judging routine like (b) of drawing 2 by it.
[0040] Therefore, since a microcomputer 7 can perform subsequent processings, without passing through a RAM clear routine by having jumped to the address of a down-stream power line period judging routine, if data are read from Interior RAM, it can operate by setting out at the time of power off.
[0041] Thus, by preparing the 1st starting address which starts an initial setting, and the 2nd starting address by which the RAM memory clear twist was also set up down-stream, and having made it make the 2nd starting address acquire at the time of discharge of a sleep mode, an initial setting can be performed for initial starting and effective data can be made usable at it at the time of power off. For this reason, for example, operation can be resumed, without [which is depended on reset of switch setting out to the time of power return] causing past [the cold] and the lack of cooling.
[0042] In addition, if a backup power supply 8 is removed and the power is turned off, since the content of the RAM memory is eliminable, it can also make it easy to return setting out to an early condition.
[0043] Moreover, with this gestalt, although the control circuit of a sherbet feeder was described, it is not limited to this. It cannot be overemphasized that it is applicable to other control equipments using a microcomputer.
[0044] Furthermore, although the operation gestalt described what used the one chip microcomputer, it is not limited to this. If data are saved at RAM at the time of power off even if it does not use an one chip microcomputer, it is clear that this approach can be used.

[0045]
[Effect of the Invention] Since this invention can make usable [after power return] the data which were effective at the time of power off by constituting as mentioned above and having made it make the 2nd starting address acquire at the time of discharge of a sleep mode, it can resume operation of a control equipment convenient.

[Translation done.]

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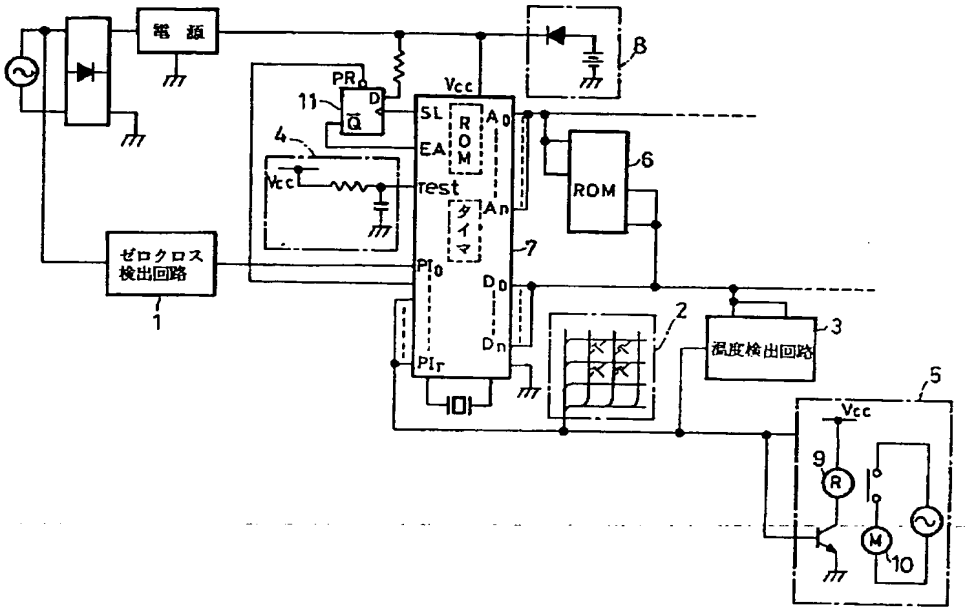
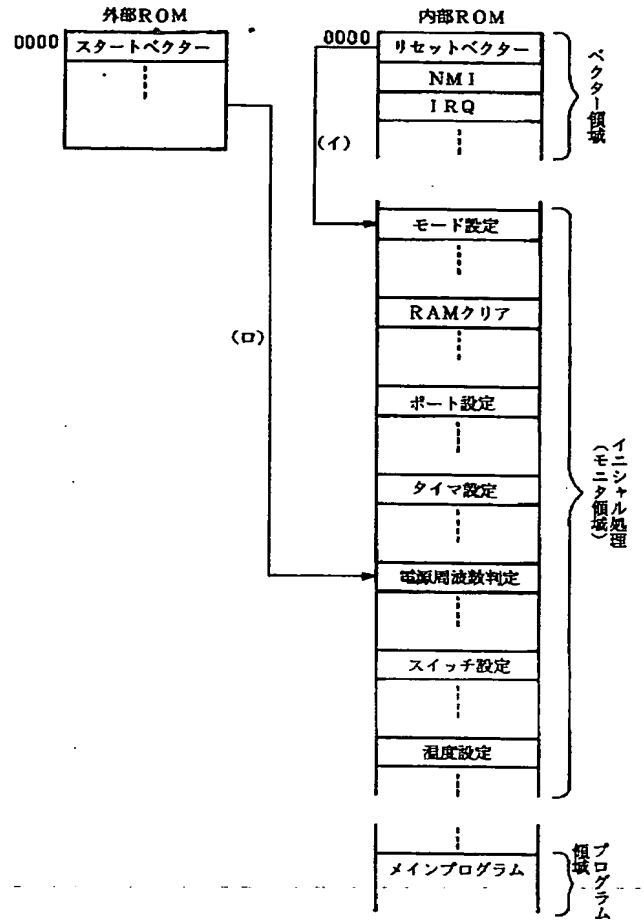
DRAWINGS

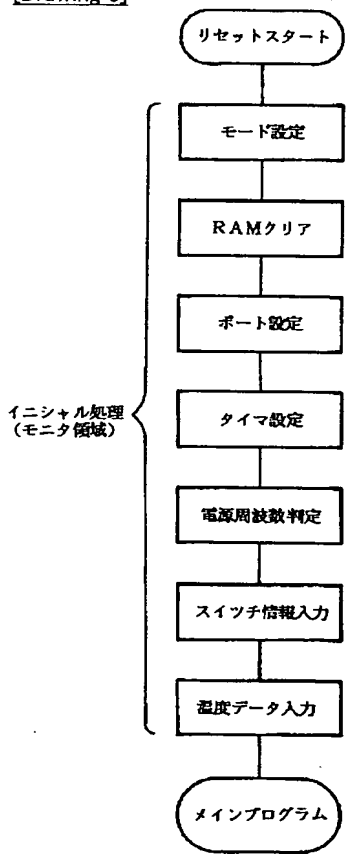
[Drawing 1]



[Drawing 2]



[Drawing 3]



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